REMARKS

Reconsideration of the above-referenced application in view of the amendments and the following remarks is respectfully requested.

Claims 1-16 were pending in this case. Applicant acknowledges that non-elected Claims 11-16 have been withdrawn from consideration and are hereby cancelled. The specification has been amended to correct various informalities relating to the identification of the drawings. New Claims 17-24 have been added.

The drawings were objected to for informalities relating to element numbers "101" and "103". Applicant has amended the specification such that modification of the drawings in response to this objection is not believed to be necessary. Similarly, the drawings were objected to for including element numbers "102" and "106a". The reference to element 102 occurs in the specification at page 10, line 21. A proposed correction to Figure 1 to remove element number 106a accompanies this paper.

Claim 9 was objected to as depending from itself. Claim 9 has been amended in response to the objection.

Claims 1, 2, 4, 5 and 7-10 stand rejected under 35 U.S.C. 103(a) as being obvious over Elder et al. (U.S. Patent No. 5,123,850) in view of Gillette et al. (U.S. Patent No. 5,831,832). Applicant respectfully traverses the rejection. Claims 1 and 10 are directed to a semiconductor device. In contrast, Elder is directed to a "non-destructive burn-in test socket for an integrated circuit die." In other words, the structure disclosed by Elder is an apparatus that is used in temporary fashion to test an integrated circuit. See Elder at col. 4, lines 37-39 where it is stated that "[w]hen testing is complete, the test socket is opened and the good die removed for assembly into a hybrid device." It is Elder's "hybrid

device", rather than the burn-in test socket, that should be compared to the claimed invention. This problem in Elder also leads to further deficiencies. For example, Claims 1 and 10 include the feature "a plurality of electrical coupling members attached to said contact pads." The contact pads are on the active surface of the integrated circuit chip. In contrast, Elder's bumps 24 are not on his semiconductor die 21, but are rather on the probe head shown in Figure 3. Claims 1 and 10 also include the feature "encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip." Elder does not teach or suggest such a feature as it would be inconsistent with the function of a burn-in test socket. The Examiner cited Gillette for its teaching of encapsulation material to cure this deficiency of Elder. However, Elder and Gillette are non-analogous art since Elder's apparatus is a burn-in test socket and Gillette's device is a plastic ball grid array package. The skilled artisan would have no motivation to take the teachings of plastic encapsulation for a semiconductor package and apply it to a burn-in test socket intended for only temporary test use. For at least these reasons, Applicant respectfully submits that Claims 1 and 10 are patentable over the cited combination of references. The same reasoning applies to Claims 2, 4, 5, and 7-9. For example, the artisan would have no reason to apply Gillette's teaching of solder balls to the invention of Elder, since Elder's apparatus is designed to be taken apart once testing is completed. Claim 7 has been amended to further define the claimed invention and to clarify that it is not a product by process claim. The cited references do not teach or suggest interdiffused coupling members and conductive lines. Applicant therefore respectfully submits that Claims 1, 2, 4, 5, and 7-10 are patentable over the cited combination of references.

Claim 3 stands rejected under 35 U.S.C. 103(a) as being obvious over Elder in view of Gillette and Akram (U.S. Patent No. 5,898,224). Applicant respectfully traverses the rejection. Claim 3 depends from Claim 1, which is

patentable over the Elder/Gillette combination for the reasons presented above. Akram is cited by the Examiner for its teaching of underfill. However, Akram does not cure the deficiencies of the Elder/Gillette combination with regard to Claim 1. Therefore, Claim 1 and Claim 3 from which it depends are both patentable over the cited combination of references.

Claim 6 stands rejected under 35 U.S.C. 103(a) as being obvious over Elder in view of Gillette and Kelly et al. (U.S. Patent No. 5,798,567). Applicant respectfully traverses the rejection. Claim 6 depends from Claim 1. In Claim 1 the conductive lines are "integral with said first surface" of the interposer. Kelly refers to "gold bonding wires" to connect an integrated circuit to a BGA substrate. The bond wires commonly used in industry are not integral with a substrate and Kelly gives no indication otherwise. Note also that Kelly does not cure the deficiencies of the Elder/Gillette combination with regard to Claim 1. Therefore, Claim 1 and Claim 6 from which it depends are both patentable over the cited combination of references.

New Claims 17-24 contain features cited above for Claims 1-10 that are not taught or suggested by the references of record. Applicant therefore respectfully requests that these new claims be passed to issuance along with Claims 1-10.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 1-10 and 17-24. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicants' attorney at the below listed telephone number and address.

Respectfully submitted,

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Version with Markings to Show Changes Made

In the Specification:

In the Section Titled:
BRIEF DESCRIPTION OF THE DRAWINGS

The specification is amended as follows:

FIG. 1 is a simplified and schematic cross section of a Ball-Grid Array device according to the invention.

FIGs. 2A to 6B [2E] show schematically both top views and cross sections of a Land-Grid array device according to the invention, at significant steps of the device assembly process.

FIGs. 2A and 2B illustrate [FIG. 2A illustrates] the IC chip with gold bumps.

FIGs. 3A and 3B illustrate [FIG. 2B illustrates] the thin film interposer.

FIGs. 4A and 4B illustrate [FIG. 2C illustrates] the process of attaching the bumped chip to the interposer.

FIGs. 5A and 5B illustrate [FIG. 2D illustrates] the process of encapsulating by overmold.

FIGs. 6A and 6B illustrate [FIG. 2E illustrates] the process of encapsulating by glob top.

In the Section Titled:
DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The specification is amended as follows:

FIG. 1 illustrates, in schematic and simplified fashion, the cross section through a device according to the

invention, generally designated 100, in the configuration of a Ball-Grid Array package. The invention, however, is generic; this means, slight variations in processing (discussed below) can specialize the device as a Land-Grid array, Pad-Grid Array, or modified Pin-Grid Array).

The device 100 is depicted as having a low profile package. As defined herein, the term "profile" refers to the thickness or height of the integrated circuit package. This definition does include the height of the solder balls before they are reflown in board attachment. The invention applies to devices of any outline, including to those having a chip-scale or chip-size package outline. As defined herein, the term "outline" relates to the overall width and length of the integrated circuit (IC) package of the present invention. The outline of the package is also referred to as the footprint of the package, because it defines the surface area on a wiring or assembly board that the package will occupy. The invention relates to packages of all sizes or ratios of chip outline versus package outline. Consequently, the invention also relates to small outline packages such as so-called chip-scale and chip-size packages.

In FIG. 1, the Ball-Grid Array chip-scale device 100 is shown with a structure similar to the MicroStarJunior™ package fabricated by Texas Instruments, Dallas, Texas, U.S.A. An important part of this package is the thin-film interposer 101. This baseline polymer film [101] (for example, polyimide) is punched with an outline needed for accommodating the number of contact "lands" of "solder balls" serving the attachment to outside parts. For some devices, this means adding typically less than 20 % to the outline of the silicon chip area. For some other device types, the baseline film may have to be substantially larger

than the chip outline to accommodate large pin-count chips. The interposer [baseline film] 101 is made of electrically insulating materials such as polyimide, preferably in the thickness range from about 40 to 80 μm; in some instances, it may be thicker. Other suitable materials include Kapton™, Upilex™, PCB resin, FR-4 (which is an epoxy resin), or a cyanate ester resin (sometimes reinforced with a woven glass cloth). These materials are commercially available from several sources; as examples, in the U.S.A., companies include 3-M, DuPont, and Sheldahl; in Japan, Shinko, Shindo, Sumitomo, and Mitsui, and Ube Industries Ltd; and in Hong Kong, Compass.

The interposer 101 has a first surface 101a and a second surface 101b. On the first surface 101a is an adhesive layer 102, and adhering to it is the metal foil 103. A plurality of electrically conductive lines is formed from foil 103. In addition, other structures of passive electrical components could be formed from this foil. Examples are resistors, inductors, distributed components, and a network of passive components and interconnected structures. It is within the scope of the invention that at least portions of these passive structures (for instance, inductors and capacitors) may be positioned under the IC chip.

The thickness of the metal foil 103 is preferably between about 15 and 40 μm. Preferred foil materials include copper, copper alloys, gold, silver, palladium, platinum, and stacked layers of nickel/gold and nickel/palladium. The thickness of the adhesive layer 102 is typically between 8 and 15 μm. The number and the width of the metal lines is, obviously, a function of the number and the pitch of the coupling members attached to the contact pads of the chip. If the metal lines are fabricated

from a foil, etching is the preferred method of production. If [It] the metal lines are deposited, a plate-up process is advantageous.

The IC chip 104 has an outline and a profile, which determine in first order the outline and profile of device 100. The chip profile (thickness) may vary from 130 to 375 μm; the majority of chips presently falls in the 250 to 375 μm thickness range. The chip outline may vary from about 0.2 to 22 mm. The package outline may vary from about 1.5 mm per side (for square-shaped chips) to 50 mm; elongated or rectangular-shaped chips and packages are common.

Chip 104 has an active surface 104a and a passive surface 104b. Active components, forming the IC, are fabricated in active surface 104a, including a plurality of contact pads 105. Dependent on the many different semiconductor device types, to which this invention is applicable, the number of contact pads varies widely, from 3 to more than 3000. Presently, the majority of chips has contact pads numbering in the 30 to 600 range.

While the present invention can be applied to any pitch of the contact pads 105, it is important to the invention that the contact pads 105 may be spaced apart from each other by less than 100 μm, center to center. In other words, while the invention applies to any, even relatively low pin count of the devices, the full impact and benefit of the invention is revealed in the category of relatively high and very high pin count devices. In a flip-chip arrangement, these contact pads can utilize the whole chip area for input/output purposes. Due to these fine-pitch contact pads, the chip area required even for a high number of inputs/outputs can be kept to a minimum.

The electrical coupling members 106 attached to these contact pads are adjusted for the small pad pitch.

Preferably, the coupling members are metal bumps selected from a group consisting of gold, copper, copper alloy, or layered copper/nickel/palladium. Another option is z-axis conductive epoxy. The bumps may have various shapes, for example rectangular, square, round, or half-dome. The cross section of bump 106 in Fig. 1 applies to several shape options of these coupling members.

Deposition methods for gold bumps on conventional aluminum metallization of the chip contact pads have been described in the technical literature. The most common method is electroplating; however, electroless deposition is also used. Deposition methods of bumps on the more recent copper metallization of the chip contact pads are preferring layered bumps, such as copper/nickel/palladium. Successful techniques have been described in U.S. Patent Applications # 60/183,405, filed on 02/18/2000 (Stierman et al., "Structure and Method for Bond Pads of Copper-Metallized Integrated Circuits"), and # 09/611,623, filed on 07/07/2000 (Shen et al., "Integrated Circuit with Bonding Layer over Active Circuitry"). The methods of these Applications are hereby incorporated by reference.

The method of attaching the coupling members 106 to the conductive lines formed from metal foil 103 is a thermo-compression bonding technique based on metal interdiffusion, as has been practiced previously in the tape-automated-bonding (TAB) fabrication method. The preferred technique for the present invention is a gang-bonding technique for array assembly. This technique has the advantage of fast and low-cost operation while resulting in high quality, reliable attachments. The automated apparatus is commercially available from Shinkawa Corporation, Japan.

As indicated in FIG. 1, the electrically insulating thin-film interposer 101 has a plurality of electrically

conductive paths 107 extending through the interposer 101, from its first surface 101a to its second surface 101b. These paths are created by opening vias through interposer 101 (using an etching, laser, or punching technique) and filling these vias either with solderable metal or solder. A suitable fabrication method has been described in U.S. Patent Application TI-31014, submitted on 10/31/2000 (Pritchett et al., "Plastic Chip-Scale Package having Integrated Passive Components"), which is hereby incorporated by reference.

The conductive paths 107 contact the conductive lines 103 at the interfaces 107a. At the second surface 101b of the interposer 101, the paths 107 form exit ports 107b. As FIG. 1 shows for Ball-Grid Array devices, there may be solder balls 108 attached to these exit ports 107b. For Land-Grid Array devices, these solder balls would not be necessary.

As defined herein, the term solder "ball" does not necessarily imply that the solder contacts are necessarily spherical. They may have various forms, such as semispherical, half-dome, truncated cone, or generally bump. The exact shape is a function of the deposition technique (such as evaporation, plating, or prefabricated units), reflow technique (such as infrared or radiant heat), and material composition. Solder balls may be selected from a group consisting of pure tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds.

As shown in FIG. 1, it is an important aspect of the present invention to create a composite structure having rigidity by encapsulating chip 104 and at least a portion of the adjacent interposer 101 [103]. The embodiment of FIG. 1 illustrates the example of an overmolded device. Using

well-known transfer molding techniques and molding compounds (usually an epoxy base material of suitable polymerization characteristics, glass transition temperature, and stabilizing inorganic fillers), the encapsulation 109 is created with a thickness appropriate for the desired profile of the overall device. For Land-Grid Array packages, the device profile is in the range from about 0.2 to 1.0 mm, for Ball-Grid Array packages, as shown in FIG. 1, the thickness of the attached solder material has to be added.

In the embodiment of FIG. 1, the encapsulation surrounds and protects the passive surface 104b of chip 104 and all area of the first interposer surface 101a with its integrated electrically conductive lines formed from metal foil 103. In another embodiment of the invention, shown in FIGs. 6A and 6B [FIG. 2E], a glob top encapsulation covers only a central portion of the device, yet enough area to provide stability to the device.

FIG. 1 illustrates the option to underfill the bump-attached chip with material 110. The preferred choice for the underfill material 110 is a non-conductive, adhesive polymer such as an insulating, adhesive thermoplastic/ thermosetting blend without conductive fillers/particles. An example are epoxy-based potting materials available from vendors such as Hitachi Chemical, Toshiba Chemical, and Namics, all of Japan.

The method of fabricating an embodiment of the present invention is illustrated in FIGs. 2A to 6B [2E] for a schematic Land-Grid Array structure. Each significant process step is shown by both a (simplified) top view and a (simplified) cross sectional view.

FIGs. 2A and 2B depict [FIG. 2A depicts] a top view and a cross section of an IC chip 201 with coupling members 202 (for example, gold bumps) attached. The chip as depicted in

FIGs. 2A and 2B [FIG. 2A] has been formed by a number of preceding process steps, which are well established in the industry and therefore not shown in FIGs. 2A and 2B [FIG. 2A]. These process steps are performed on a whole semiconductor wafer in a wafer fab. For the present invention, the following process steps are especially significant:

* Depositing an electrical coupling member of gold, copper, or copper/nickel/palladium on each contact pad of each IC chip on the wafer, each chip having pads spaced apart by less than 100 μm, center to center. The contact pads of the IC are located on active surface 201a of the chip.
* mounting the semiconductor wafer on a mounting tape, held tight in a solid frame, in preparation for chip singulation (sawing);
* sawing the wafer into discrete chips; and
* UV curing the mounting tape for releasing the sawed chips from the mounting tape.

FIGs. 3A and 3B depict [FIG. 2B depicts] a top view and a cross section of an electrically insulating thin-film interposer as prepared from the materials and process steps explained above. In particular, the electrically insulating film 210 has a plurality of electrically conductive paths 211 through the thickness of the interposer from the first surface 210a to the second surface 210b, further a plurality of electrically conductive lines 212 on the first surface. The interposer further has a plurality of patterned attachment sites 213 on the first surface, which match the pattern of the coupling members (gold bumps) on the IC chip. The fabrication steps of the thin-film interposer include the following major steps:

* Depositing and patterning a plurality of electrically

conductive lines 212 and attachment sites 213 on the first surface 210a of the interposer; and

* forming a plurality of electrically conductive paths 211 through the interposer. These paths 211 are contacting the conductive lines at the first interposer surface (211a) and form exit ports on the second interposer surface (211b).

FIGs. 4A and 4B illustrate [FIG. 2C illustrates] the assembly process step of IC chip and interposer. The top view of FIG. 4A [2C] shows the passive surface 201b of the chip after assembly onto the interposer 210, while the active chip surface 201a faces the first surface 210a of the interposer (flip-chip assembly). This important process step comprises:

* assembling the active chip surface 201a onto the first interposer surface 210a such that each of the chip coupling members 202 is aligned and brought into contact with the respective attachment site 213 of the interposer; and
* using thermo-compression gang bonding, all contact connections are created essentially concurrently by metal interdiffusion. A chip-size portion of the interposer is thus covered by the assembled chip 201.

An optional process step comprises:

* Underfilling an adhesive polymer 220 into any spaces under the chip between the chip coupling members 202; these spaces have been formed by the process step of assembling chip 201 onto the interposer 210. The underfill material strengthens the assembly.

In a variation of the above process flow, the underfill material may be applied prior to the thermo-compression bonding process step.

FIGs. 5A, 5B, 6A, and 6B [2D and 2E] illustrate the important process step of encapsulating the assembled device for creating a composite structure having rigidity. The process step comprises:

* Encapsulating, with a polymer compound, the passive surface 201b of the chip and at least a portion of the first interposer surface 210a which is not covered by the attached chip.

** If a transfer molding method is used, the molding compound 231 protects the first interposer surface 210a completely (FIGs. 5A and 5B [FIG. 2D]). The outline of the molding compound thus defines the outline of the device. Transfer molding, including mold compound curing, is the preferred method, since it is a well-established and low-cost (batch process) technology.

** If a protection method by a glob top is used, the polymer material 232 covers only a portion of the first interposer surface 210a which is not covered by the attached chip. That surface portion is marked 240 in FIGs. 6A and 6B [FIG. 2E]. The glob top may be round, as shown in FIGs. 6A and 6B [FIG. 2E], or have any other desired outline (for instance, square or rectangular).

After the step of encapsulating follows the step of:

* separating the resulting composite structure into discrete units. A preferred method is sawing. The resulting device outline may be that of a generic Ball-Grid Array device, or a more specific chip-scale or chip-size device.

The final devices as depicted in FIGs. 5A, 5B, 6A, and 6B [2D and 2E] belong into the category of Land-Grid Array devices. In order to fabricate a Ball-Grid Array device, an additional process step is performed as:

* attaching solder balls to the exit ports 211b on the second interposer surface 210b. Preferably, this process step is performed, before the above step of separating is executed.

The following process steps are analogous to known fabrication techniques:

- Marking;
- Testing;
- Visual/mechanical inspecting;
- Interposer editing;
- Packing; and
- Shipping.

While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. As an example, the method of providing gold bumps to the IC chip for connection to the interposer may be replaced by a method of providing a z-axis conductive epoxy. As another example, the interposer may comprise two or three layers of electrically insulating and conductive materials. As yet another example, the semiconductor chip material may be silicon, silicon germanium, gallium arsenide, or any other semiconductor material employed for mass production. It is therefore intended that the appended claims encompass any such modifications or embodiments.

In the Claims:

Please amend the claims as follows:

1. A semiconductor device comprising:
   an integrated circuit chip having an outline, active and passive surfaces, and active components including a plurality of contact pads, spaced apart by less than 100 μm center to center, on said active surface;
   a plurality of electrical coupling members attached to said contact pads, said coupling members selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy;
   an electrically insulating thin-film interposer having first and second surfaces, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface;
   said chip coupling members attached to said conductive lines, covering an area portion of said first interposer surface; and
   encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.
2. The device according to Claim 1 further having solder balls attached to said exit ports on said second interposer surface.
3. The device according to Claim 1 further having an

adhesive non-conductive polymer underfilling any spaces between said chip coupling members attached to said conductive lines under said chip.

4. The device according to Claim 1 wherein said interposer is a polyimide film.

5. The device according to Claim 1 wherein said interposer has an outline larger than said outline of said chip.

6. The device according to Claim 1 wherein said electrically conductive lines are made of a material selected from a group consisting of copper, copper alloy, or copper plated with tin, tin alloy, silver, or gold.

7. (amended) The device according to Claim 1 wherein said coupling member is interdiffused with said conductive lines [attachment is provided by metal interdiffusion of thermo-compression bonding].

8. The device according to Claim 1 wherein said encapsulation material is a molding compound.

9. (amended) The device according to Claim 8 [9] wherein said molding compound has the same outline as said interposer.

10. A semiconductor device comprising:

an integrated circuit chip having an outline, active and passive surfaces, and active components including a plurality of contact pads on said active surface;

a plurality of electrical coupling members attached to said contact pads, said coupling members selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy;

an electrically insulating thin-film interposer having first and second surfaces, a plurality of

electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface;

said chip coupling members attached to said conductive lines, covering an area portion of said first interposer surface; and

encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

Please cancel Claims 11-16.

Please add the following new claims.

17. (new) A semiconductor device comprising:

an integrated circuit chip having an outline, active and passive surfaces, and active components including a plurality of contact pads on said active surface;

a plurality of electrical coupling members attached to said contact pads;

an electrically insulating thin-film interposer having first and second surfaces, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface;

said chip coupling members interdiffused with said conductive lines; and

encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

18. (new) The device according to Claim 17 further having solder balls attached to said exit ports on said second interposer surface.

19. (new) The device according to Claim 17 further having an adhesive non-conductive polymer underfilling any spaces between said chip coupling members attached to said conductive lines under said chip.

20. (new) The device according to Claim 17 wherein said interposer is a polyimide film.

21. (new) The device according to Claim 17 wherein said interposer has an outline larger than said outline of said chip.

22. (new) The device according to Claim 17 wherein said electrically conductive lines are made of a material selected from a group consisting of copper, copper alloy, or copper plated with tin, tin alloy, silver, or gold.

23. (new) The device according to Claim 17 wherein said encapsulation material is a molding compound.

24. (new) The device according to Claim 23 wherein said molding compound has the same outline as said interposer.

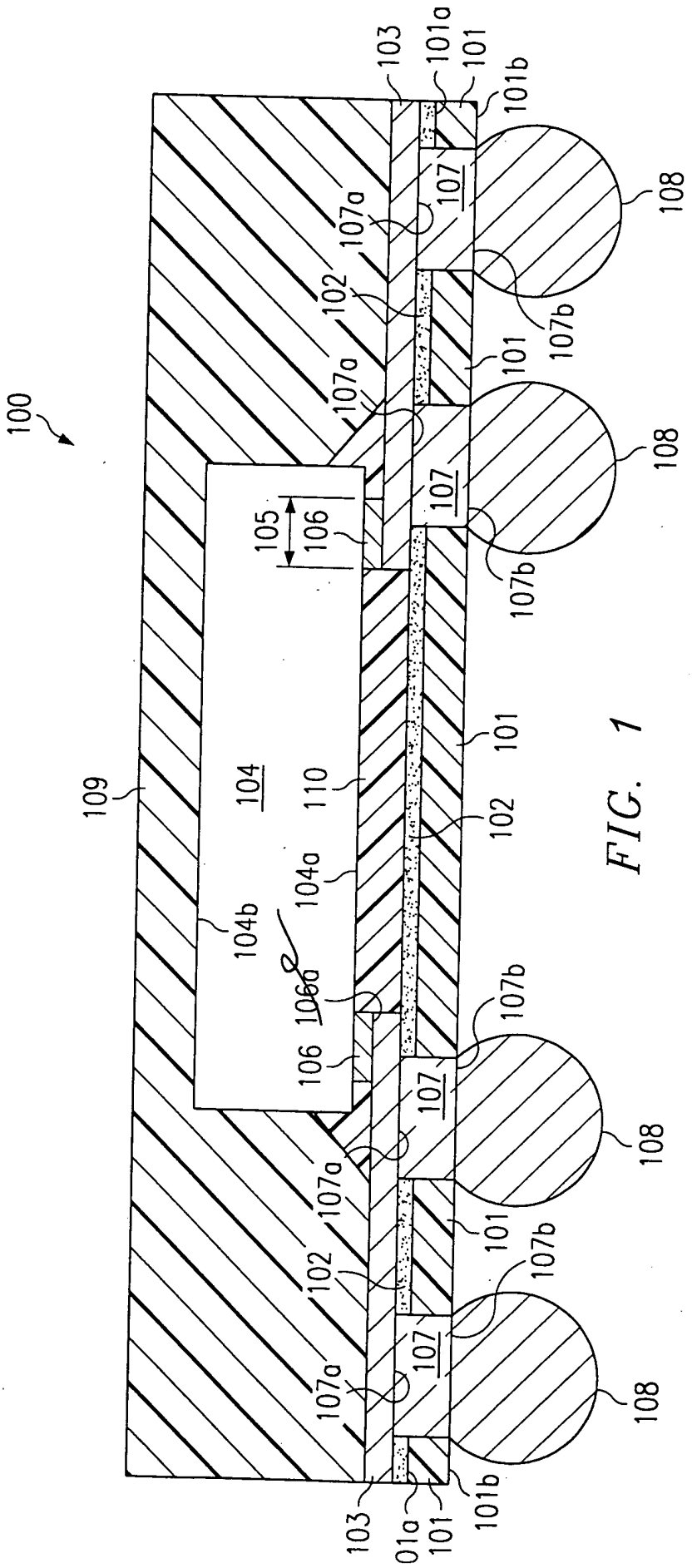

FIG. 1